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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,532	09/24/2004	Bhupendra SHARMA	TI-38242	5531

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,532	SHARMA ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-10* is/are allowed.

6)☒ Claim(s) *1-5 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to papers filed 05/15/06. The rejection in previous office action is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiguchi et al. (USP 5275393).

As to claim 1, Horigushi et al.'s figure 10 shows a bias generation circuit (101) generating a bias current for a circuit portion (the remain elements in figure 10) containing a plurality of transistors of a low voltage specifications the circuit portion operating using a first supply voltage (Vcc), wherein the first supply voltage is greater than the low voltage specification, the bias generation circuit comprising: a primary current block (2) generating a primary bias current using a second supply voltage (V2), wherein the second supply voltage is less than the first supply voltage (figures 4 and 5); a backup current block (1) generating a backup bias current using the first supply voltage (Vcc) (see figure 4); and a mulliplexor (3) selects one of the primo bias current and the backup bias current as the bias current.

As to claim 2, figure 10 shows that the multiplexor selects the backup bias current as the bias current when the second supply voltage is not present (when V2 is lower than V1).

As to claim 3, figure 2 shows that the multiplexor performs the selecting according to a select signal (output of 4) connected to a node, wherein the primary current block comprises a first current source (it is inherent that voltage generating circuit has current source) and the backup current block comprises a second current source, wherein the first current source and the second current source drive the node.

Claim 11 recites similar limitations of claim 1. Therefore, it is rejected for the same reasons.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (USP 5275393) in view of Yamauchi (USP 5982162) (previously cited).

Horiguchi et al.'s figure 10 shows all limitations of the claim except for the detail of circuit 1. Yamauchi's figure 3 shows a voltage step down circuit that generates a constant voltage independent of external power supply. Therefore, it would have been obvious to one having ordinary skill in the art to use Yamauchi's voltage step down circuit to generate Horiguchi et al.'s V1 for the purpose of improving the circuit performance. Thus, the modified Horiguchi et al.'s figure 10 further shows that the second current source comprises: a resistor (Yamauchi's 25) connected between the first supply voltage and a first node; a first NMOS

transistor (Yamauchi's 29); and a second NMOS transistor (Yamauchi's 31); wherein the drain terminal of the first NMOS transistor is connected to its gate and the first node; the drain terminal of the second NMOS transistor is connected to the node; the gate terminal of the second NMOS transistor is connected to the gate of the first NMOS transistor, and the source of the second NMOS transistor is connected to the source of the first NMOS transistor.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (USP 5275393) in view of Yamauchi (USP 5982162) and Wang (USP 5939933).

The modified Horiguchi et al.'s figure 10 shows all limitations of the claim, except for the detail of Yamauchi's current source. However, Wang's figure 4 shows a current source circuit (all elements except for circuit 22) that generates precision current. Therefore, it would have been obvious to one having ordinary skill in the art to use Wang's current source for Yamauchi's current source for the purpose of generating precision current source. Thus, the modified Horiguchi et al.'s figure 1 shows that the backup current source further comprises current mirror circuit.

Allowable Subject Matter

6. Claims 6-10 are allowed.

Claims 6-10 are be allowable because the prior art fails to teach or suggest a device having processor, DAC, filter and line driver, wherein the line driver comprises the current selecting circuit as claimed.

Response to Arguments

7. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that Horiguchi et al. fails to teach "a primary current block generating a primary bias current using a second supply voltage, wherein said second supply voltage is less than said first supply voltage". The Examiner respectfully disagrees. As stated in the rejection of claim 1, Vcc is considered as the claimed "first supply voltage". Horiguchi et al.'s figure 5 clearly shows that V2 (second supply voltage) is less than first supply voltage (Vcc).

Applicant further argues "Horiguchi et al. teaches completely opposite of what the Examiner has stated. According to Horiguchi, et al. as long as the external supply voltage Vcc (V) stays within 5+/- 0.5 volts, Vl = Vl and when the Vcc reaches 6 volts, Vl = V2. Thus, the higher voltage than in ordinary operation is impressed on the internal voltage, so that the voltage aging of the internal circuit be conducted." (col. 7, lines 29-56, figure 2b). Accordingly, Horiguchi et al. teach completely opposite of what is recited in claims 1-2 and therefore, does not anticipate claims 1-2". The Examiner respectfully disagrees. The rejection above consider V1 as backup voltage, wherein Vi is generated buy using first voltage Vcc. Horiguchi et al. teaches the higher of V1 and V2 is selected to output 3. Thus, when V2 is lower (not present or not available), the backup voltage V1 is selected.

Applicant further argues "switch 3 receives a control signal from comparator 4 and it is not connected to a node". The Examiner respectfully disagrees. The output of comparator 4 is a node. Thus, the control signal from the comparator is connected to the node.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

June 15, 2006